R18

Code No: 153AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, December - 2024 /January - 2025

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ITE, CE(SE), CSE(CS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Sketch V-I characteristics of a semiconductor junction diode for both silicon and germanium diodes. Indicate differences, if any, in the characteristics curve of the two types. [2]

b) Briefly describe Static Resistance. [3]

c) Define the following transistor ratings: [2]
i) Forward Current Gain ii) Thermal Runaway.

d) Draw the frequency response of an RC -Couple amplifier. [3]

e) Write short notes on voltage variable resistance. [2]

f) Write the Truth table of Universal gates. [3]

g) State and prove DeMorgan laws. [2]

h) Simplify the Boolean expression to a minimum number of literals:
$f = (x + y)(x + y')$. [3]

i) Define FLIP-FLOP. [2]

j) Define Random-Access Memory. [3]

PART – B

(50 Marks)

2.a) Show the basic PN-diode action diagrammatically, when it is
i) Unbiased ii) Reverse-biased iii) Forward-biased.

b) With neat input and output waveforms, explain the working of Bridge Rectifier. [5+5]

OR

3.a) Explain the principle of operation of a LED.

b) What is a clipper? With the help of circuit diagram and waveforms describe the operation of positive and negative clippers. [4+6]

4.a) Draw the circuit diagram of an NPN junction transistor CE configuration and describe the static input and output characteristics. Also, define active, saturation and cutoff regions, and saturation resistance of a CE transistor.

b) Derive an expression for the stability factor of a collector-to-base bias circuit. [5+5]

OR

5.a) Consider a common emitter NPN transistor with fixed bias. If $\beta = 80$, $R_B = 390\ k\Omega$, $R_C = 1.5k\Omega$ and $V_{CC} = 30$ V, find the coordinates of the Q-Point.

b) With neat circuit diagram explain the working of RC coupled amplifier. [5+5]

6.a) Explain the construction and working of N-Channel depletion type MOSFET.

b) Explain the working of basic NAND DTL gate with neat circuit diagram. [5+5]

OR

7.a) Define the following parameters of the JFET:
i) Transconductance ii) Drain resistance iii) Amplification factor.

b) With neat circuit diagram, explain the working of basic RTL gate. [5+5]

8.a) Simplify the Boolean function by first finding the essential prime implicants.
$F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$.

b) Implement the boolean function on suitable multiplexer.
$F(a, b, c) = \sum (1, 3, 5, 6)$. [5+5]

OR

9.a) Design a Binary Full Adder with minimum number of NAND gates.

b) Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use block diagrams for the three multiplexers. [5+5]

10.a) Explain the working of shift registers in SIPO Mode.

b) Write short notes on the following:
i) Latches ii) state reduction iii) Read-Only Memory. [5+5]

OR

11.a) Design a 4-bit ripple counter and draw the timing diagram.

b) With neat logic diagram, explain the working of NAND SR Flip flop. [5+5]

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